

HIT 2 690-07

Prior Application: I. ARAI et al
Serial No. 08/438,911
Filed: May 10, 1995

Group Art Unit: 2775
Examiner: C. Nguyen
For: IMAGE DISPLAY APPARATUS

Box: Patent Application
Assistant Commissioner of Patents
Washington, D.C. 20231

This is a request for filing a continuation application under 37 C.F.R. 1.53(b) of pending prior application Serial No. 08/438,911, filed on May 10, 1995, entitled IMAGE DISPLAY APPARATUS, by all of the inventors named in the prior application.

- CLAIMS AS FILED IN THE PRIOR APPLICATION
LESS ANY CLAIMS CANCELED BY AMENDMENT BELOW
PLUS ANY CLAIMS ADDED BY ACCOMPANYING PRELIMINARY AMENDMENT

3. A check including the amount of \$690.00 is enclosed to cover the Filing Fee.

4. Cancel claims 2-15 before calculating the Filing Fee.

5. Amend the specification by inserting, before the first line:

--This is a continuation application of U.S. Serial No. 08/438,911, filed on May 10, 1995; which is a divisional application of U.S. Serial No. 08/013,810, filed February 2, 1993.--

6. New drawings are enclosed, ten (10) sheets, Figs. 1-10.

7. The power of attorney is set forth in the Declaration in the prior application or an associate power of attorney is hereby granted to:

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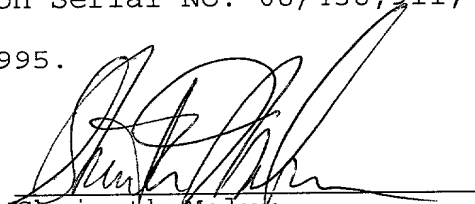
8. The prior application is assigned to Hitachi, Ltd.

9. Priority of the following Japanese patent application is claimed under 35 U.S.C. § 119:

No. 04-069320, filed February 20, 1992.

The certified priority document has been filed in prior application Serial No. 08/013,810.

The undersigned hereby declares that no matter contained in the specification, including the claims, and drawings filed in the present continuation application would have been new matter in the prior application Serial No. 08/438,911, as originally filed on May 10, 1995.



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Date: February 7, 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Accompanying Continuation Application under
37 CFR 1.53(b) :

Prior Application: I. ARAI et al
Serial No. 08/438,911
Filed: May 10, 1995

Group Art Unit: 2775
Examiner: C. Nguyen
For: IMAGE DISPLAY APPARATUS

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above application
as follows.

IN THE CLAIMS

Please cancel claim 1 and add new claims 16-20 as set
forth below.

--16. A display unit which receives a video signal and a
synchronization signal from a computer, and which displays an
image in accordance with the video signal and the
synchronization signal on a screen, the display unit
comprising:

an interface circuit which receives a control signal
which is generated by a program that is previously programmed
by a computer for operating a computer body; and

a memory which stores control data concerning display control, the stored control data is read out by the control signal from the interface circuit;

wherein the displayed image is adjusted in accordance with the control data which is read out from the memory.

--17. A display unit which receives a video signal and a synchronization signal from a computer, and which displays an image in accordance with the video signal and the synchronization signal on a screen, the display unit comprising:

an interface circuit which receives the video signal and the synchronization signal and a control signal which is generated by a program that is previously programmed by a computer for operating a computer body;

a video circuit which is connected to the interface circuit and receives the video signal from the interface circuit;

a driving circuit which is connected to the interface circuit and receives the synchronization signal from the interface circuit;

a display device which is driven by signals from the video and driving circuits to generate the displayed image;

a memory which stores control data concerning display control, the stored control data is read out by the control signal from the interface circuit;

wherein the displayed image is adjusted in accordance with the control data which is read out from the memory.

--18. A display unit according to claim 16, wherein the video signal carries digital image data.

--19. A display unit for receiving a video signal and a synchronization signal from a computer, and for displaying an image in accordance with the video signal and the synchronization signal on a screen, the display unit comprising:

interface means for receiving a control signal which is generated by a program that is previously programmed by a computer for operating a computer body; and

memory means for storing control data concerning display control, the stored control data is read out by the control signal from the interface means;

wherein the displayed image is adjusted in accordance with the control data which is read out from the memory means.

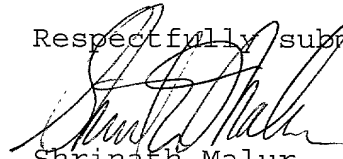
--20. A display unit according to claim 19, wherein the video signal carries digital image data.--

REMARKS

Claim 1 has been canceled. New claims 16-20 have been added. Accordingly, claims 16-20 are currently pending in the application.

Examination is respectfully requested.

Respectfully submitted,



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1 BACKGROUND OF THE INVENTION

The present invention relates to an image display apparatus including an input unit such as a keyboard, a computer body and a display unit, and more particularly to an image display apparatus in which a display size, a display position and brightness of a picture in the display unit can be adjusted by the input unit such as the keyboard through the computer body to improve the handling capability. The image display apparatus of the present invention can be used in a work station and an advanced personal computer using a display unit.

At present, in the display units for a computer terminal, the display position and size of the picture and a deflection frequency of a video signal to be displayed are variously different. Accordingly, one display unit for the computer terminal is designed to be able to treat various video signals.

The display unit of this type employs a microcomputer and an LSI memory to provide an optimum picture display for each kind of video signals. Such a display unit in a prior art is disclosed in Japanese Patent Unexamined Publication No. 1-321475, for example.

This conventional display unit is directed to a multi-scan type CRT display unit, which includes a

1 memory in which information relative to display
positions and sizes of the picture is stored for each
kind of video signals and which is controlled by a
microcomputer in that display unit. The information
5 relative to the optimum display position and size of the
picture in accordance with an input video signal is read
out from the memory and a deflection circuit of the
display unit is controlled by the read-out information.
Further, when a video signal inputted in the display
10 unit is not known, the memory stores no information
relative to the inputted video signal and accordingly
adjustment switches disposed on a front panel of the
display unit are operated without the intervention of
the computer so that information for adjusting the
15 display position and the display size of the picture is
inputted. A control circuit such as the microcomputer
prepares information for control including deflection
and makes adjustment.

In the prior art described above, the display
20 unit is designed to obtain the optimum picture display
in accordance with the input video signal, while, in
another prior art, a display state is controlled to be
switched from the computer body in accordance with the
variety of the multi-media. Such a display unit in the
25 prior art is disclosed in Japanese Patent Unexamined
Publication No. 2-60193.

This conventional display unit is directed to
a CRT display apparatus used in display of an electronic

1 apparatus such as a personal computer and which can
switch the number of scanning lines between 200 lines
and 400 lines freely and be shared by a television
receiver.

5 More particularly, in the above prior art, the
computer body produces a discrimination signal super-
posed on an video signal during a blanking period and
the display unit switches the deflection frequency on
the basis of the discrimination signal.

10 In the former prior art (Publication No. 1-
321475) of the above two prior arts, since the display
position and size of the picture are all controlled by
the display unit, it is necessary for the operator to
separate his fingers from the input unit such as the
15 keyboard connected to the computer body and extend his
hands to the adjustment switches of the display unit
disposed at a separate location to operate the switches
when the adjustment of the display position and size of
the picture are required. Accordingly, it is trouble-
20 some in the handling capability.

Further, in the latter prior art (Publication
No. 2-60193), the display state is controlled by the
input unit such as the keyboard connected to the
computer body, while since only the deflection frequency
25 can be switched only by a binary value, there is a
problem that only two specific signals can be treated
and a sufficient display state required by the user of
the computer can not be obtained.

1 SUMMARY OF THE INVENTION

It is a primary object of the present invention to solve the problems in the prior arts by providing an image display apparatus capable of adjusting a display picture by an input unit such as a keyboard near at hand through a computer body without extending the hands to adjustment switches of a display unit and obtaining a display state required by the user exactly.

10 It is another object of the present invention to improve the operability in a computer system and the handling capability of the image display apparatus.

It is still another object of the present invention to provide an image display apparatus capable of adjusting a display picture from a computer body by using a conventional circuit without the provision of a new circuit.

In order to solve the above problems, according to the present invention, in a general computer system, a computer body comprises addition means for adding a control signal for a display picture to a video signal or a synchronizing signal and a display unit comprises separation means for separating the added control signal and control means for adjusting the display state on the basis of the separated control signal.

Alternatively, the computer body comprises preparation means for preparing the control signal to produce it with a predetermined system and the display

1 unit comprises control means for receiving the control signal to adjust the display state on the basis of the control signal.

Alternatively, the computer body comprises
5 display processing means for producing the prepared image data and the control signal for the display picture in the form of a digital signal to the display unit and the display unit comprises control means for preparing an analog video signal and synchronizing
10 signal from the image data and producing an adjustment signal for adjusting a predetermined location of the display unit on the basis of the control signal.

Alternatively, the computer body comprises modulation means for adding the control signal for the
15 display picture to an AC power supply for operating the computer body and the display unit comprises demodulation means for separating the modulated control signal and control means for adjusting an internal circuit of the display unit by the control signal from the demodulation means to obtain a predetermined display picture.
20

Further alternatively, the control signal from the input unit such as the keyboard is received by the display unit as it is and the display unit comprises instruction identification means for identifying the
25 control signal relative to the adjustment of the display picture and control means for adjusting the display picture on the basis of a signal from the instruction identification means.

1 The addition means of the computer body adds
the control signal for the display unit to the video
signal or the synchronizing signal produced by the
computer body when the instruction inputted by the input
5 unit such as the keyboard relates to the adjustment of
the display picture of the display unit. In the display
unit, the separation means takes out the added control
signal and the control means adjusts the internal cir-
cuit of the display unit in accordance with the control
10 signal to thereby display a predetermined picture.

 Alternatively, the preparation means prepares
a control signal in accordance with the control signal
for the display picture from the input unit such as the
keyboard and produces it through an exclusive connection
15 line, and when the control means of the display unit
receives the control signal, the control means adjusts a
predetermined portion of the internal circuit of the
display unit in accordance with the control signal and
adjusts the display picture.

20 Alternatively, the display processing means
processes a drawing instruction prepared by a CPU in the
computer body to prepare image data for displaying a
video signal and prepare a control signal for the
display picture, so that the image data and the control
25 signal are produced to the display unit with a predeter-
mined system for transmission and reception of a digital
signal. Further, the control means receives the image
data and the control signal from the display processing

1 means and prepares the video signal, the synchronizing
signal and the adjustment signal for the internal
circuit of the display unit.

Alternatively, the modulation means prepares
5 the control signal for the display picture from the
information or instruction relative to the adjustment of
the display picture and adds the control signal to the
AC power supply for the computer body to transmit the
control signal. The demodulation means extracts the
10 control signal added by the modulation means. The
control means adjusts a predetermined portion of the
internal circuit of the display unit on the basis of the
control signal from the demodulation means to adjust the
display picture.

15 Further alternatively, the instruction
identification means identifies a signal relative to the
adjustment of the display picture from signals directly
inputted by the input unit such as the keyboard to
prepares the control signal for adjustment. The control
20 means adjusts the predetermined portion of the internal
circuit of the display unit in accordance with the con-
trol signal from the instruction identification means to
adjust the display picture.

BRIEF DESCRIPTION OF THE DRAWINGS

25 Preferred embodiments of the present invention
will now be described in conjunction with the accompany-
ing drawings, in which:

1 Fig. 1 is a block diagram schematically illustrating a first embodiment of an image display apparatus according to the present invention;

 Fig. 2 is a block diagram schematically illustrating an actual example of a control signal addition
5 circuit and a display control circuit shown in Fig. 1;

 Fig. 3 is a waveform diagram of signals of Fig. 2;

 Fig. 4 is a block diagram schematically illustrating an actual example of a control signal separation
10 circuit and the display control circuit shown in Fig. 1;

 Fig. 5 is a waveform diagram of signals of Fig. 4;

 Fig. 6 is a block diagram schematically illustrating another actual example of the control signal
15 addition circuit and the display control circuit shown in Fig. 1;

 Fig. 7 is a block diagram schematically illustrating a second embodiment of an image display
20 apparatus according to the present invention;

 Fig. 8 is a block diagram schematically illustrating a third embodiment of an image display apparatus according to the present invention;

 Fig. 9 is a block diagram schematically illustrating a fourth embodiment of an image display
25 apparatus according to the present invention; and

 Fig. 10 is a block diagram schematically illustrating a fifth embodiment of an image display

1 apparatus according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram schematically illustrating a first embodiment of an image display apparatus according to the present invention. In Fig. 1, numeral 1a denotes a computer body, in which numeral 11 a CPU, 12 an input unit interface connected to the computer body 1a for processing various instruction signals inputted from a first input unit 10 (which transmits a user's intention to the computer) such as a keyboard, a mouse, a pen for input, 13 a memory circuit constituting a main memory, 14 an input/output port for connection with a peripheral device not shown, 15 a display control circuit for producing a video signal and a synchronizing signal for driving a display unit, 16 a control signal addition circuit for superposing or adding a control signal to the video signal or the synchronizing signal produced by the display control circuit 15, and 17 an external memory constituted by a floppy disk, a hard disk or a memory card which is disposed separately from the memory circuit 13. Further, numeral 1b denotes a display unit, in which numeral 18 denotes a control signal separation circuit for extracting the control signal from the video signal or the synchronizing signal on which the control signal produced by the control signal addition circuit 16 is superposed, 19 a first display control circuit for producing an adjustment

1 signal for a predetermined circuit on the basis of the
control signal extracted by the control signal separa-
tion circuit 18, 20 a video circuit, 21 a deflection
circuit constituting display drive means, and 22 a
5 cathode ray tube for displaying a video signal.

Operation of Fig. 1 is now described. In the
computer body 1a, other portions except the control
signal addition circuit 16 are the same as the general
configuration of a conventional personal computer or
10 work station.

When the user of the computer inputs a control
instruction for adjustment of the display picture in the
display unit 1b by means of a first input unit 10 such
as a keyboard, a mouse, a pen for input connected to the
15 computer body 1a, the input unit interface 12 converts
the control instruction into a digital signal, which is
recognized by the CPU 11 which controls the control
signal addition circuit 16.

The control signal addition circuit 16 pre-
20 pares a control signal Sc in accordance with the control
instruction. The control signal Sc for the display unit
1b is superposed during the vertical retrace period on
the video signal R, G or B or the synchronizing signal
for display produced by the display control circuit 15.
25 The signal on which the control signal Sc is superposed
is represented with the prime ('). The control signal
Sc is prepared in accordance with the control instruc-
tion inputted in the input unit 10.

1 The control signal separation circuit 18 of
the display unit 1b separates the added control signal
Sc from the video signal R, G or B or the synchronizing
signal Hs or Vs produced by the control signal addition
5 circuit 16 to supply it the first display control
circuit 19 and supplies the video signals R, G and B to
the video circuit 20 and the synchronizing signals Hs
and Vs to the deflection circuit 21, respectively.

 The first display control circuit 19 produces
10 adjustment signals Sa and Sb for the video circuit 20
and the deflection circuit 21 on the basis of the
inputted control signal Sc, respectively, and supplies
the signals Sa and Sb to the video circuit 20 and the
deflection circuit 21, respectively, to adjust them.

15 In this way, the display picture is adjusted,
so that the user's desired picture is displayed in the
cathode ray tube 22.

 Fig. 2 is a block diagram schematically illus-
trating an actual example of the control signal addition
20 circuit 16 of Fig. 1 and Fig. 3 is a waveform diagram
illustrating waveforms of signals in Fig. 2.

 In Fig. 2, numeral 161 denotes an address
decoder, 162 a data latch circuit, 163 an edge detection
circuit for detecting an edge of a pulse, 164 a shift
25 register circuit, 165 and 170 AND circuits, 166 a level
conversion circuit for converting a level of a signal,
167 an analog switch, 168 a counter circuit for counting
17 clock pulses, and 169 a set and reset type flip-flop

1 circuit (hereinafter, referred to as an RSFF circuit).

Operation of Fig. 2 is now described.

As described above, when the user of the
computer inputs the control instruction for adjustment
5 of the display picture of the display unit 1b by means
of the input unit 10 connected to the computer 1a, the
input unit interface 12 supplies the control instruction
to the CPU 11 through a computer bus BUS. Then, the CPU
11 recognizes the control instruction and supplies a
10 control data C_D to the control signal addition circuit
16 through the computer bus BUS.

The address decoder 161 supplies the control
data C_D to the data latch circuit 162 when the control
data supplied to the decoder is a control data for
15 adjusting the display picture of the display unit 1b.
Then, the edge detection circuit 163 detects a leading
edge of the vertical synchronizing signal V_s by means of
the horizontal synchronizing signal H_s and supplies the
edge detection pulse P_e to the shift register circuit
20 164, the counter circuit 168 and the RSFF circuit 169.

The counter circuit 168 is supplied with the
edge detection pulse P_e as a reset signal and with the
horizontal synchronizing signal H_s as a clock signal and
starts its counting operation in response to the rising
25 edge of the clock signal. When the counter circuit 168
counts 17 clocks after input of the reset signal, the
counter circuit produces a carry output signal S_{ca} which
is supplied to a reset input terminal of the RSFF

1 circuit 169. Thus, the RSFF circuit 169 produces a V
gate pulse P_v as shown in Fig. 3. The control signal Sc
for the display unit 1b is superposed during a high
level period T_H of the V gate pulse P_v .

5 On the other hand, the shift register circuit
164 reads the control data C_D held in the data latch
circuit 162 in response to the edge detection pulse Pe
supplied from the edge detection circuit 163. The shift
register circuit 164 performs the shift operation in
10 response to the clock signal constituted by the hori-
zontal synchronizing signal Hs produced from the AND
circuit 170 during the high level period T_H of the V
gate pulse to produce the control data C_D' shown in Fig.
3.

15 Further, the control data C_D' is supplied to
the AND circuit 165 which produces a logical product of
the control data C_D' and the horizontal synchronizing
signal Hs . The output signal of the AND circuit is
converted into a video signal level by the level
20 conversion circuit 166 to be supplied to the switch
circuit 167. Other input of the switch circuit 167 is
supplied with a B (blue) video signal directly without
being processed, and the switch circuit 167 selects the
output of the level conversion circuit 166 during the
25 high level period T_H and the B video signal during other
low level period T_L by using the V gate pulse P_v as a
change-over control signal for the switch to be able to
obtain a B' video signal on which the control signal is

1 added as shown in Fig. 3. In the embodiment, the
control signal Sc is added to the B video signal having
a low visual sensitivity of color, while the control
signal may be added to other R (red) or G (green) visual
5 signal or the synchronizing signal Hs or Vs.

Fig. 4 is a block diagram schematically illus-
trating a first embodiment of the control signal sepa-
ration circuit 18 and the first display control circuit
19 of Fig. 1 and Fig. 5 is a waveform diagram showing
10 waveforms of signals in Fig. 4.

In Fig. 4, numeral 401 denotes a distributor,
402 a low pass filter (hereinafter referred to as an
LPF), 403 a level conversion circuit, 404 and 405
buffers, 406 a divide-by-17 counter or 17-step counter,
15 407 an RSFF circuit, 408 and 409 AND circuits, 410 an
inverter, 411 a 16-stage shift register, 412 a decoder
circuit, 413 a D/A conversion circuit (hereinafter
referred to as a D/AC), and 414 an edge detection
circuit.

20 Operation of Fig. 4 is now described with
reference to Fig. 5.

The B' video signal from the control signal
addition circuit 16 is supplied to the distributor 401
which divides the video signal into two signals, one of
25 which is supplied to the video circuit 20 shown in Fig.
1 together with other video signals R and G and the
other of which is supplied to the LPF 402. With the B'
video signal supplied to the LPF 402, an unnecessary

1 frequency component such as noise contained in the B' video signal is removed in the LPF 402 and the B' video signal is then converted into a digital signal level in the level conversion circuit 403.

5 Further, the vertical synchronizing signal Vs is supplied through the buffer 404 to the edge detection circuit 414, in which the leading edge thereof is detected and is supplied to the 17-step counter 406, the RSFF circuit 407 and the 16-stage shift register 411 as
10 an edge detection pulse 418 shown in Fig. 5.

When the 17-step counter circuit 406 is reset by the edge detection pulse 418, the 17-step counter circuit 406 starts its counting operation for the horizontal synchronizing signal Hs supplied through the
15 buffer 405 as a clock signal. Thus, when rising edges of 17 clocks are counted, the counter circuit produces a 17-clock detection pulse. The RSFF circuit 407 is set by the edge detection pulse 418 and reset by the 17-clock detection pulse to produce the V gate pulse 419
20 shown in Fig. 5.

The AND circuit 408 takes a logical product of an output signal of the level conversion circuit 403 and the V gate pulse of the RSFF circuit 407 to extract the control signal 420 added to the B' video signal.
25 Further, the other AND circuit 409 takes a logical product of the V gate pulse and the horizontal synchronizing signal Hs produced by the buffer 405 and inverted by the inverter 410 to produce a clock signal for the

1 16-stage shift register 411 and the D/AC (D/A Converter)
413.

The 16-stage shift register 411 is reset by
the edge detection pulse 418 to clear the held contents
5 thereof and successively holds the control signal 420 in
response to the clock signal from the AND circuit 409.
The decoder circuit 412 decodes four held values at the
first, second, fifteenth and sixteenth stages of the 16-
stage shift register 411, and when the decoder circuit
10 detects the start bit and the stop bit in the control
signal 420, the decoder circuit produces a load pulse
422 for the D/AC 413. Further, the output signal from
the second-stage of the shift register 411 is used as a
serial data 421 of the D/AC 413 shown in Fig. 5.

15 The D/AC 413, which is a serial input and
multi-channel D/A converter, selects any of a plurality
of D/A converters included therein in accordance with
D/AC control address in the serial data 421 shown in
Fig. 5 and updates the D/A converted output value in
20 accordance with a value of the control data portion. At
this time, the serial data 421 is successively taken in
the D/AC 413 in synchronism with the clock signal from
the AND circuit 409 and is settled by the rising edge
(UP) of the load pulse from the decoder 412.

25 Thus, the video circuit 20 and the deflection
circuit 21 shown in Fig. 1 can be adjusted by an adjust-
ment voltage or current produced from the D/AC 413 as an
adjustment signal.

1 Fig. 6 is a block diagram schematically illus-
trating a second actual example of the control signal
separation circuit 18 and the display control circuit 19
of Fig. 1. In Fig. 6, numeral 601 denotes a selector,
5 602 a one-chip microcomputer, and 603 a writable read-
only memory (hereinafter referred to as EEPROM (Electric
Erasable Programmable Read Only Memory)). Other
elements having the same number as in Fig. 4 have the
same function.

10 Operation of Fig. 6 is now described.

 The operation that the control signal Sc added
to the B' video signal is separated by the AND circuit
408 and the clock signal for writing of the shift
register 411 is prepared by the AND circuit 409 is quite
15 the same operation as that of Fig. 4. In the second
example, the microcomputer 602 is used to process the
control signal to the display unit 1b sent from the
computer body 1a shown in Fig. 1.

 First of all, usually, the microcomputer 602
20 controls the selector 601 to select the clock signal for
writing from the AND circuit 409 and write the control
signal in the shift register circuit 411. At this time,
the edge detection pulse from the edge detection circuit
414 is supplied to the microcomputer 602 as an interrupt
25 signal 418 and after a predetermined time the microcom-
puter 602 controls the selector 601 by a selector
control signal Ss to select the clock signal S_{CL} for
reading from the microcomputer 602.

1 The control signal held in the shift register
circuit 411 is successively read out in response to the
clock signal S_{CL} for reading from the microcomputer 602
and is supplied to the microcomputer 602. When the
5 signal supplied to the microcomputer is the correct
control signal, the microcomputer 602 produces the
control data to supply it to the D/AC 413 to thereby
adjust a predetermined circuit in the display unit 1b.
Further, the control data is also written in the EEPROM
10 603. Thus, when the display unit 1b is next turned on,
the control data is read out from the EEPROM 603 to
perform the predetermined adjustment.

 Further, in the second example, by previously
storing the control data in the EEPROM 603, a necessary
15 control data can be read out in accordance with the
control signal S_c from the computer body 1a. Accord-
ingly, the control information for the display unit 1b
can be previously programmed in the software for
operating the computer body in addition to the control
20 information from the input unit 10, so that a predeter-
mined adjustment can be made for each software.

 As described above, in the first embodiment of
the present invention, the control signal is added to
the video signal or the synchronizing signal during the
25 vertical retrace period, while a DC level itself of the
video signal can be used as the control signal. In this
case, the control signal separation circuit 18 may
reproduce the DC level of the video signal and adjust

1 the predetermined circuit of the display unit 1b in
accordance with a voltage value of the DC level.
Further, in the first embodiment, the video circuit 20
and the deflection circuit 21 of the display unit 1b are
5 adjusted, while a high-voltage circuit portion can be
naturally controlled to adjust the focus or the like.

Fig. 7 is a block diagram schematically
illustrating a second embodiment of the present
invention. In Fig. 7, numeral 1c denotes a computer
10 body different from the computer body shown in Fig. 1
and in the computer body 1c, numeral 70 denotes a
control signal preparation circuit. Further, numeral 1d
denotes a display unit different from the display unit
shown in Fig. 1 and in the display unit 1d, numeral 71
15 denotes a second display control circuit different from
the first display control circuit 19 shown in Fig. 1.
Other elements designated by the same numerals as those
of Fig. 1 have the same function as that of the elements
of Fig. 1.

20 Operation of Fig. 7 is now described briefly.

In Fig. 7, the video signal and the synchro-
nizing signal are produced by the display control
circuit 15 in the same manner as in a general personal
computer or work station.

25 When the user of the computer inputs the
control instruction for adjusting the display picture of
the display unit 1d by means of the input unit 10 con-
nected to the computer body 1c, the control instruction

1 is sent to the control signal preparation circuit 70
through the input unit interface 12, the CPU 11 and the
computer bus BUS.

The control signal preparation circuit 70
5 holds the control instruction and prepares the control
signal corresponding to the control instruction to
produce it to the display unit 1d at a proper timing.
An output system of the control signal at this time can
use an existing interface such as, for example, RS-232C,
10 GP-IB and SCSI. Accordingly, the control signal pre-
paration circuit 70 includes the interface circuit.

The second display control circuit 71 of the
display unit 1d receives the control signal produced by
the control signal preparation circuit 70 through the
15 same interface circuit as that included in the control
signal preparation circuit 70 and produces the adjust-
ment voltage or current for the video circuit 20 and the
deflection circuit 21 as the adjustment signal on the
basis of the received control signal to adjust the video
20 circuit 20 and the deflection circuit 21.

In the second embodiment of the present
invention, since the control signal is transmitted and
received by means of the general-purpose interface, bi-
directional communication between the display unit 1d
25 and the computer body 1c can be made. Accordingly, the
computer body can recognize whether the display unit 1d
has received the control signal exactly or not, how the
control state of the display unit 1d at the current time

1 is or whether the display unit 1d is exactly operated or not.

Fig. 8 is a block diagram schematically illustrating a third embodiment of the present invention. In Fig. 8, numeral 1e represents a computer body different from that of Figs. 1 and 7 and in the computer body 1e, numeral 81 represents a display processing circuit for preparing an image data for a display image, and 82 an interface circuit. Numeral 1f represents a display unit different from that of Figs. 1 and 7, 83 an interface circuit, and 84 a display controller for preparing various signals for driving the display unit 1f. The interface circuits (hereinafter referred to as an I/F circuit) 82 and 83 serve to transmit and receive signals between the display processing circuit 81 in the computer body 1e and the display controller 84 in the display unit 1f. Other elements having the same numerals as those of Figs. 1 and 7 have the same function.

20 Operation of Fig. 8 is now described.

An image processing instruction issued by the CPU 11 is supplied to the display processing circuit 81 through the computer bus BUS. The display processing circuit 81 receives the image processing instruction and prepares the image data for the display image.

At this time, when the user of the computer inputs the control instruction for adjusting the display picture of the display unit 1f by means of the input

1 unit 10 connected to the computer body 1e, the control
instruction is sent to the display processing circuit 81
through the input unit interface 12, the CPU 11 and the
computer bus. When the display processing circuit 81
5 receives the control instruction, the display processing
circuit 81 prepares the control signal in a predeter-
mined location other than the image data area.

The image data and the control signal thus
prepared are sent to the display unit 1f through the I/F
10 circuit 82 as the image information in accordance with a
predetermined interface specification, for example, the
SCSI standards having a large transfer rate.

In the display unit 1f, the I/F circuit 83
receives the image information from the I/F circuit 82
15 and supplies the image information to the display
controller 84 successively. The display controller 84
writes the received image information into an internal
memory successively and prepares the video signals for
R, G and B and the synchronizing signal from the image
20 data portion of the written image information. Further,
when the control signal is present in the image infor-
mation, the adjustment voltage or current as the
adjustment signals Sa' and Sb' for the video circuit 20
and the deflection circuit 21 is produced to adjust the
25 video circuit 20 and the deflection circuit 21.

In addition, when the image information
written in the internal memory of the display controller
84 is not updated within a predetermined time, the

1 display controller 84 controls the video circuit 20 to
minimize an amplitude level of the video signal, so that
the brightness of the cathode ray tube 22 is reduced to
prevent burning of the cathode ray tube 22.

5 Even in the third embodiment of the present
invention, since the interfaces between the computer
body 1e and the display unit 1f have the capability for
bidirectional communication, not only the image data and
the control signal can be transmitted from the computer
10 body 1e but also a signal for reception confirmation and
a report signal for operation situation can be trans-
mitted from the display unit 1f. Further, since the
computer body 1e is connected to the display unit 1f
through a single interface cable, the complexity of the
15 connection can be solved.

Fig. 9 is a block diagram schematically
illustrating a fourth embodiment of the present
invention. In Fig. 9, numeral 1g represents a computer
body different from that of Figs. 1, 7 and 8, and in the
20 computer body 1g, numeral 91 represents a modulation
circuit. Numeral 1h represents a display unit different
from that of Figs. 1, 7 and 8, and in the display unit
1h, numeral 92 represents a display control circuit, 93
a demodulation circuit, and 94 and 95 power plugs.
25 Other elements having the same numerals as those of Fig.
1 have the same function.

Operation of Fig. 9 is now described.

When the user of the computer inputs the

1 control instruction for adjusting the display picture of
the display unit 1h by means of the input unit 10 con-
nected to the computer body 1g, the control instruction
is supplied to the CPU 11 through the input unit inter-
5 face 12. The CPU 11 processes the control instruction
and supplies the control signal corresponding to the
control instruction to the modulation circuit 91 through
the computer bus BUS. The modulation circuit 91 modu-
lates the received control signal and superposes it to
10 the AC power to transmit the signal from the power plug
94 through a power line PL to the display unit 1h.

In the display unit 1h, when the AC power is
supplied from the power plug 95 through the power line
PL, the demodulation circuit 93 demodulates the modu-
15 lated control signal superposed on the AC power to
reproduce the original control signal. The reproduced
control signal is supplied to the display control
circuit 92. The display control circuit 92 produces the
adjustment voltage or current as the adjustment signals
20 Sa and Sb for the video circuit 20 and the deflection
circuit 21 in accordance with the contents of the
control signal to adjust the video circuit 20 and the
deflection circuit 21.

In this manner, in the embodiment, since the
25 control signal is transmitted to the display unit 1h
through the power line PL, the display unit 1h can be
controlled without increased signal line for the control
signal.

1 Fig. 10 schematically illustrates a fifth
embodiment of the present invention. The fifth embodi-
ment is now described briefly. In Fig. 10, numeral 1
represents a computer body constituted by a general
5 personal computer or work station, 1j a display unit
different from that of the preceding embodiments, 101 a
second input unit such as a keyboard, a mouse, or a pen
for unit connected to the computer body 1 and the
display unit 1j, 102 a command identification circuit in
10 the display unit, and 103 a third display control
circuit. Other elements having the same numerals as
those of Fig. 1 have the same function.

 In Fig. 10, when the user of the computer
operates the second input unit 101, an input signal such
15 as the control instruction is inputted to the computer
body 1 and the display unit 1j. The input signal input-
ted to the display unit 1j is processed by the command
identification circuit 102 and is taken out as the
display control signal when the input signal is an
20 instruction relative to the display control. The third
display control circuit 103 makes control relative to
the display operation by the control voltage or current
with respect to the associated portion of the video
circuit 20 and the deflection circuit 21 on the basis of
25 the display control signal. In the embodiment of Fig.
10, since the computer body does not prepare the control
signal for the display, there is no burden bearing upon
the CPU of the computer. In this manner, the user of

1 the computer can control the display unit by means of
the second input unit without direct contact to the
display unit. The signal line connected from the second
input unit 101 to the display unit 1j may use the signal
5 lines connected to the computer body 1 as they are or
may be an exclusive signal line for transmitting only
the display control signal. For the former case, the
input unit such as the general keyboard can be utilized
as it is. For the latter case, it is necessary to add a
10 special input unit for display control to the second
input unit. Further, a remote control circuit employing
the infrared rays or the like is used to reduce the
number of connection lines between the second input unit
101 and the display unit 1j, so that the complexity due
15 to wiring can be reduced. In the fifth embodiment, an
input unit such as a mouse, a touch panel, a pen for
input or the like can be naturally used as the input
means for the control instruction in addition to the
keyboard.

20 According to the present invention, the
following effects are attained:

- (1) The user of the computer can adjust the
display picture by the input unit such as the keyboard
near at hand through the computer body without extending
25 the hands to adjustment switches of the display unit.
- (2) The user can obtain the necessary display
state exactly.
- (3) The operability in the computer system and the

1 handling capability of the display unit are improved.

(4) The individual user can adjust the display state of the image display apparatus in accordance with circumstances.

5 (5) The adjustment of the display picture can be attained with the minimum control hardware.

(6) Standard lines can be used without the provision of new lines.

(7) The complexity due to wiring can be avoided by
10 using the remote control circuit.

(8) It is possible to automatically adjust the optimum picture to be displayed on the display unit by adjusting the operation of software by means of the control program of a display integrated into the
15 application program at the computer side, and accordingly it is unnecessary for the user to take care the adjustment of the display.

CLAIMS:

1. An image display apparatus including an input unit, a computer body and a display unit, wherein said computer body comprises addition means for preparing a control signal Sc on the basis of an control instruction inputted by said input unit for adjusting a display picture of said display unit and for adding said control signal to a video signal R, G or B or a synchronizing signal Hs or Vs produced separately for driving said display unit to be produced to said display unit, and said display unit comprises separation means for separating said added control signal from said video signal or said synchronizing signal produced by said addition means and display control means for producing an adjustment signal on the basis of said control signal produced from said separation means to adjust display drive means in said display unit.

2. An image display apparatus according to Claim 1, wherein said computer body comprises a CPU and signal generation means for producing said video signal and producing a horizontal synchronizing signal Hs and a vertical synchronizing signal Vs as said synchronizing signal, and said addition means comprises a hold circuit for holding said control instruction inputted by said input unit and supplied through said CPU, a shift register circuit for taking in contents of said hold circuit with said vertical synchronizing signal Vs as a reference, a counter circuit for counting said hori-

zontal synchronizing signal Hs by a predetermined value with said vertical synchronizing signal Vs as a reference, a gate circuit for supplying said horizontal
15 synchronizing signal as a reading clock of said shift register circuit until said counter circuit counts by the predetermined value with said vertical synchronizing signal Vs as the reference, a level conversion circuit for converting a level of a signal read out from said
20 shift register circuit into a level of said video signal produced by said signal generation means, and a selection circuit for selecting an output of said level conversion circuit during an output period of said gate circuit and selecting said video signal during other
25 period.

3. An image display apparatus according to Claim 1, wherein said display unit comprises a video circuit and a deflection circuit, and said control means comprises a plurality of digital-to-analog conversion
5 circuits, whereby a predetermined digital-to-analog conversion circuit is selected from said plurality of digital-to-analog conversion circuits on the basis of address information included in said control signal Sc produced by said separation means and control data
10 included in said control signal Sc is converted into an adjustment voltage or current as said adjustment signal by said digital-to-analog conversion circuit to adjust said video circuit and said deflection circuit.

4. An image display apparatus according to Claim

1, wherein said display unit comprises a video circuit
and a deflection circuit, and said control means com-
prises a microcomputer, a nonvolatile memory and a
5 plurality of digital-to-analog conversion circuits,
wherein when a power supply of said display unit is
turned on, control information stored in said non-
volatile memory is read out by said microcomputer to be
supplied to a predetermined circuit of said plurality of
10 digital-to-analog conversion circuits so that said video
circuit and said deflection circuit are adjusted by an
output of said digital-to-analog circuit, and when said
control signal Sc is produced by said separation means,
said control signal is processed by said microcomputer
15 to be supplied to a predetermined circuit of said
plurality of digital-to-analog conversion circuits so
that said video circuit and said deflection circuit are
adjusted by an output of said digital-to-analog conver-
sion circuit and said control signal is written in said
20 nonvolatile memory as said information.

5. An image display apparatus according to Claim
1, wherein said addition means adds said prepared con-
trol signal Sc to said separately produced video signal
R, G or B during a vertical blanking period.

6. An image display apparatus including an input
unit, a computer body and a display unit, wherein said
computer body comprises preparation means for preparing
a control signal Sc on the basis of an control instruc-
5 tion inputted by said input unit for adjusting a display

picture of said display unit to produce said control
signal to said display unit, and said display unit
comprises control means for producing an adjustment
signal on the basis of said control signal produced by
10 said preparation means to adjust display drive means in
said display unit.

7. An image display unit according to Claim 6,
wherein delivery of said control signal Sc from said
computer body and said preparation means to said control
means in said display unit is made by means of a
5 general-purpose interface, said preparation means
comprising signal input means, said control means com-
prising signal output means, information relative to
operation situation of said display unit capable of
being transmitted through said interface from said
10 display unit to said computer body.

8. An image display apparatus including an input
unit, a computer body and a display unit, wherein said
computer body comprises display processing means for
preparing a control signal Sc on the basis of an control
5 instruction inputted by said input unit for adjusting a
display picture of said display unit to produce said
control signal to said display unit together with image
data produced separately for displaying an image in said
display unit, and said display unit comprises control
10 means for preparing video signals R, G and B and syn-
chronizing signals Hs and Vs on the basis of said image
data produced by said display processing means and for

producing an adjustment signal on the basis of said control signal produced by said display processing means
15 to adjust display drive means in said display unit.

9. An image display apparatus according to Claim 8, wherein said control means controls said display drive means in said display unit to set said display unit to be a non-display state or a state near said non-
5 display state when said image data produced by said display processing means is not updated during a pre-determined time.

10. An image display apparatus including an input unit, a computer body and a display unit, wherein said computer body comprises modulation means for preparing a control signal Sc on the basis of an control instruction
5 inputted by said input unit for adjusting a display picture of said display unit and modulating said control signal to add said control signal to an AC power supply PL, and said display unit comprises demodulation means for separating said added control signal Sc from said AC
10 power supply PL to demodulate said control signal and control means for producing an adjustment signal on the basis of said control signal Sc produced by said demodulation means to adjust display drive means, in said display unit.

11. An image display apparatus including a second input unit, a computer body and a display unit, wherein said computer body and said display unit are supplied with a part or all of instructions inputted by said

5 second input unit, and said display unit comprises
preparation means for preparing a control signal Sc on
the basis of said control instruction to produce it when
an instruction inputted by said input unit is a control
instruction for adjusting a display picture of said
10 display unit and control means for producing an adjust-
ment signal on the basis of said control signal Sc
produced by said preparation means to adjust display
drive means in said display unit.

12. An image display apparatus according to Claim
11, wherein said second input unit includes an exclusive
input portion for inputting said control signal exclu-
sively, and an instruction inputted by said exclusive
5 input portion is supplied to at least said display unit.

13. An image display apparatus according to Claim
11, wherein transmission of said instruction from said
second input unit to said display unit is made by means
of infrared rays or radio waves to thereby reduce the
5 number of connection lines between said input unit and
said display unit.

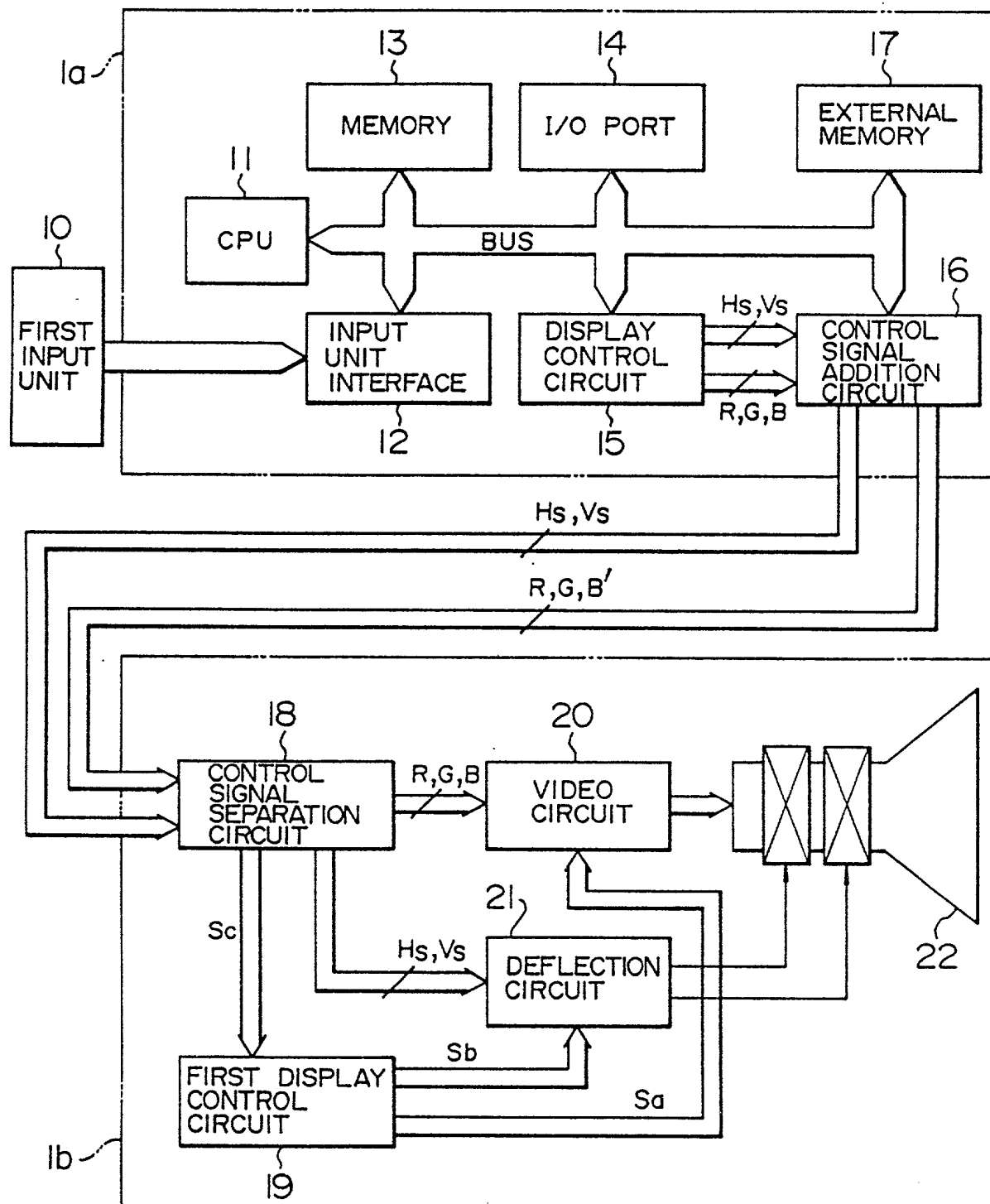
14. An image display apparatus according to Claim
1, wherein said input unit includes a keyboard, a mouse
and a pen for unit.

15. An image display apparatus according to Claim
11, wherein said input unit includes a keyboard, a mouse
and a pen for unit.

ABSTRACT OF THE DISCLOSURE

An image display apparatus capable of adjusting a display picture by an input unit through a computer body is disclosed. When the user inputs a control instruction for adjusting the display picture of the display unit by the input unit connected to the computer body, a control signal addition circuit prepares a control signal S_c corresponding to the control instruction and adds the control signal to a video signal R , G or B or a synchronizing signal H_s or V_s produced by a display control circuit during a vertical retrace period. A control signal separation circuit separates the added control signal S_c from the video signal R , G or B or the synchronizing signal H_s or V_s produced by the control signal addition circuit. A display control circuit produces adjustment signals S_a and S_b on the basis of the control signal from the control signal separation circuit to adjust a video circuit and a deflection circuit. Thus, the user can adjust the display picture by the input unit near at hand without extending the hands to adjustment switches of the display unit.

FIG. 1



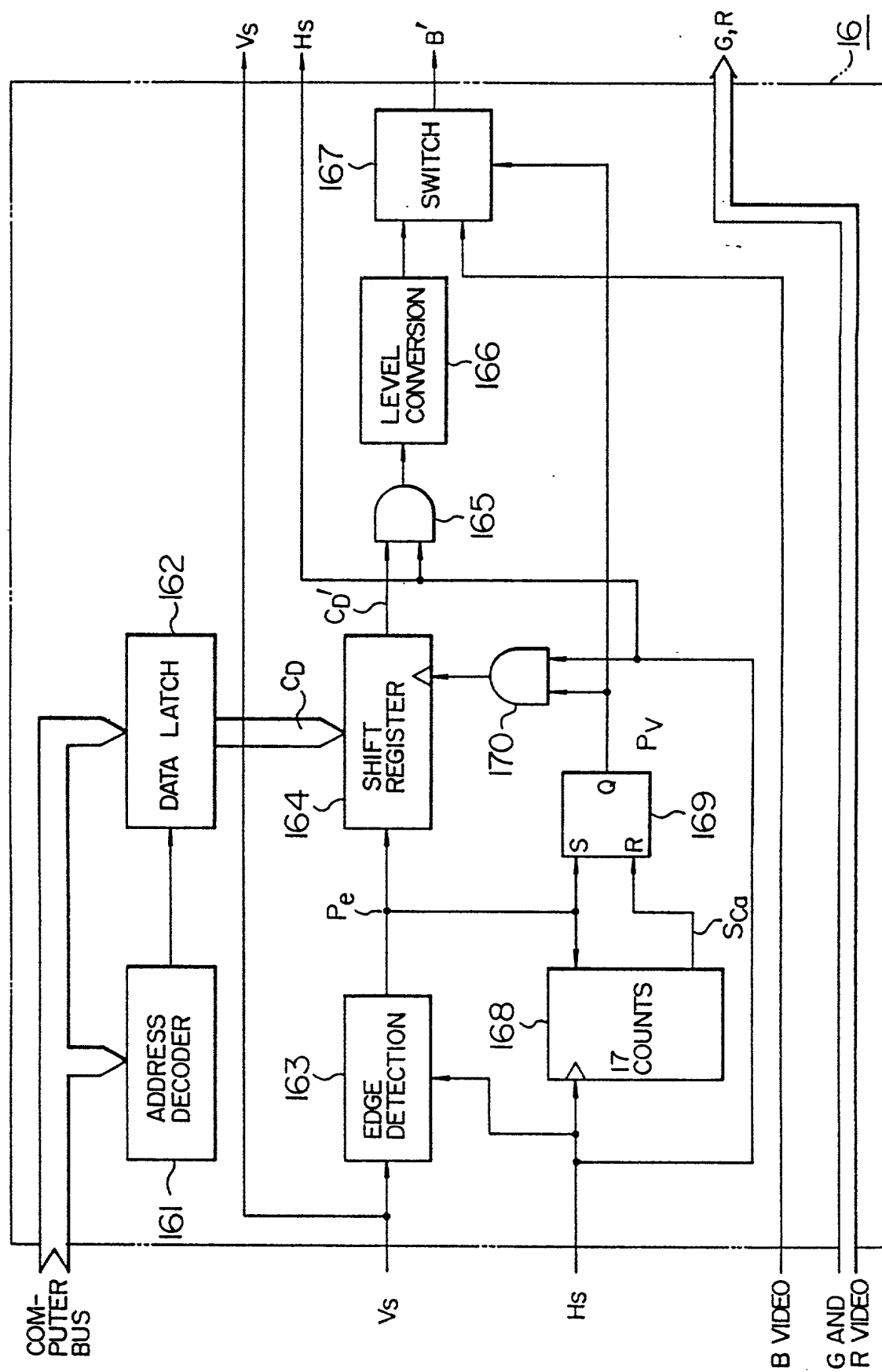
[illegible]

FIG. 3

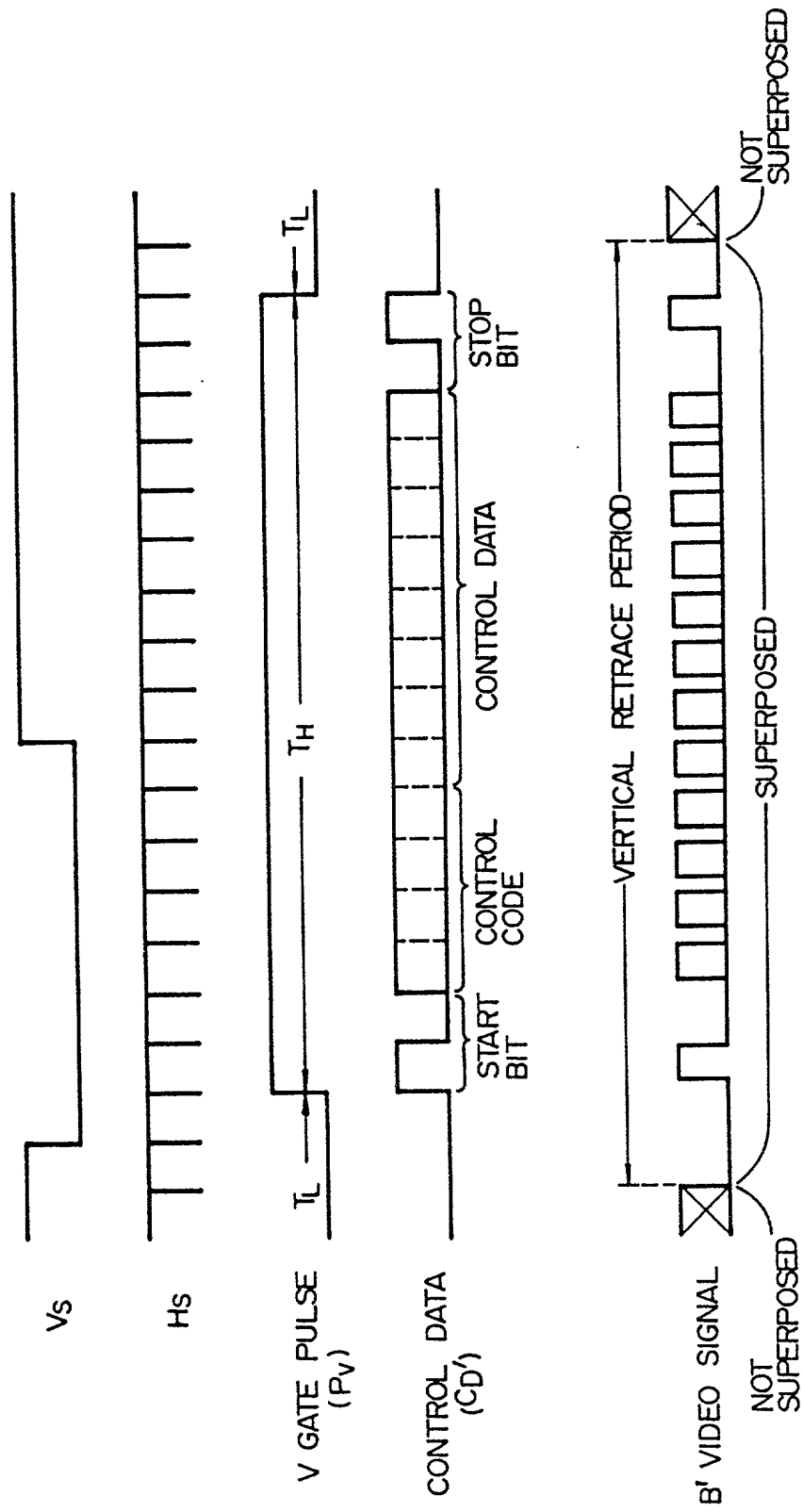


FIG. 4

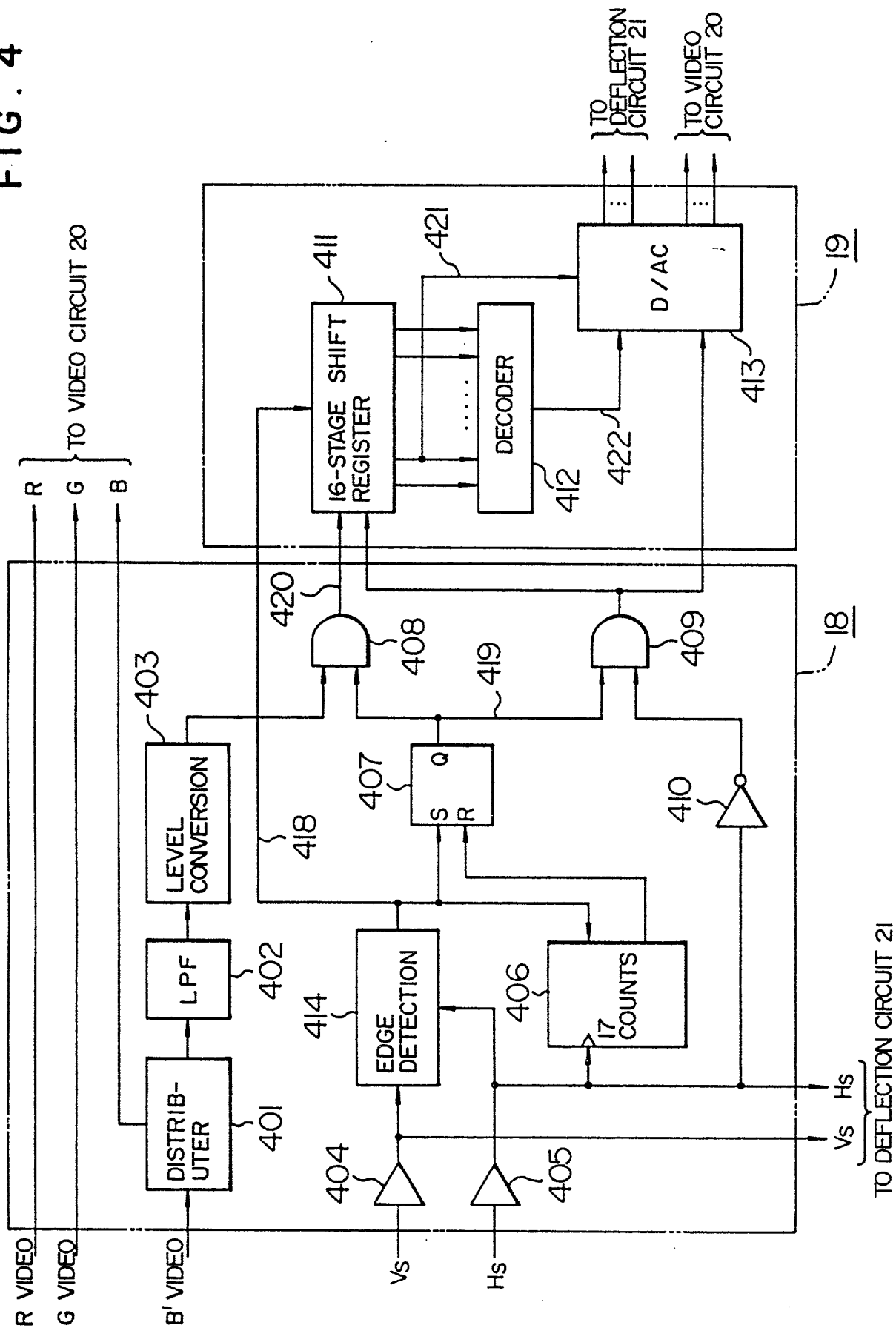


FIG. 5

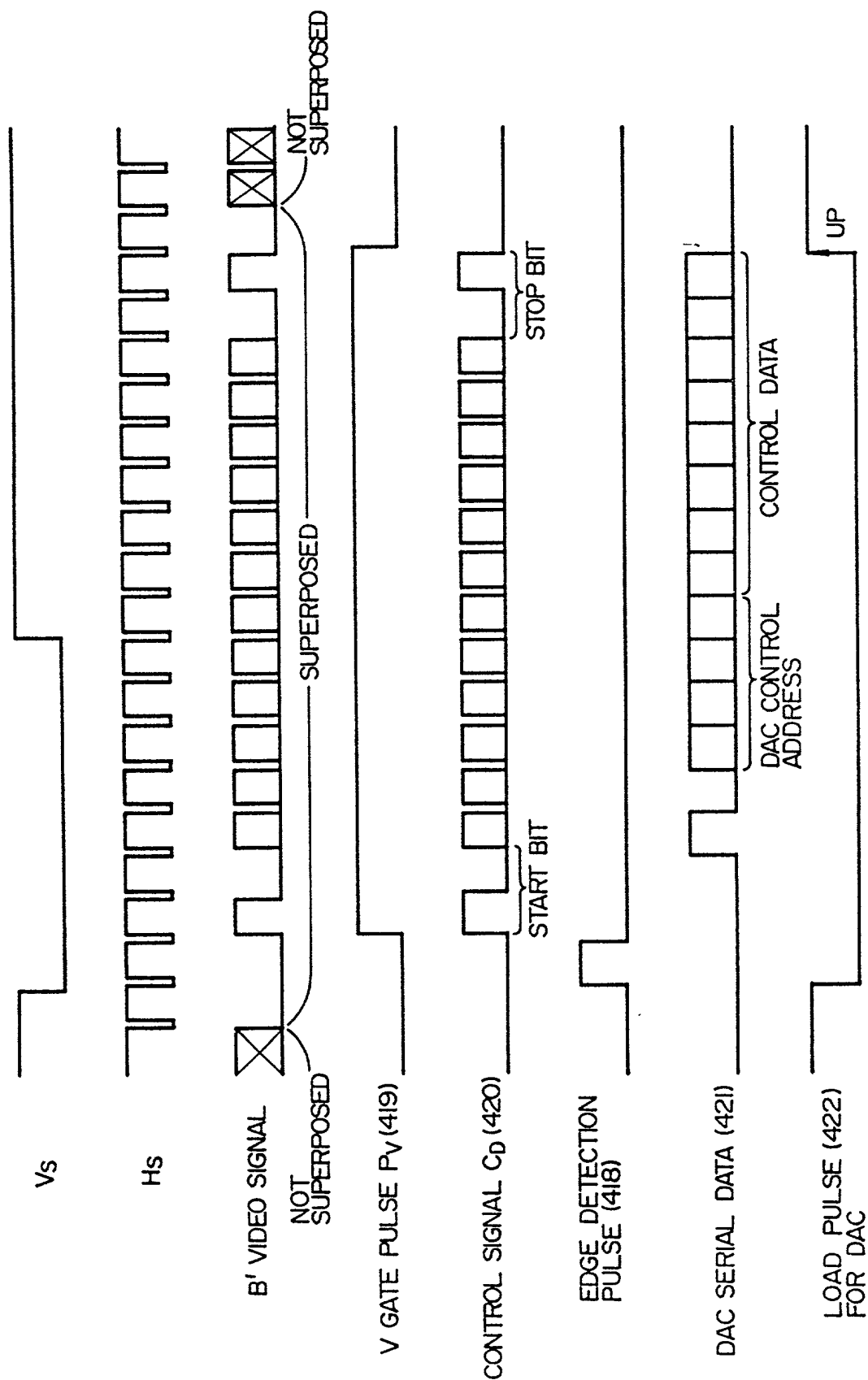


FIG. 6

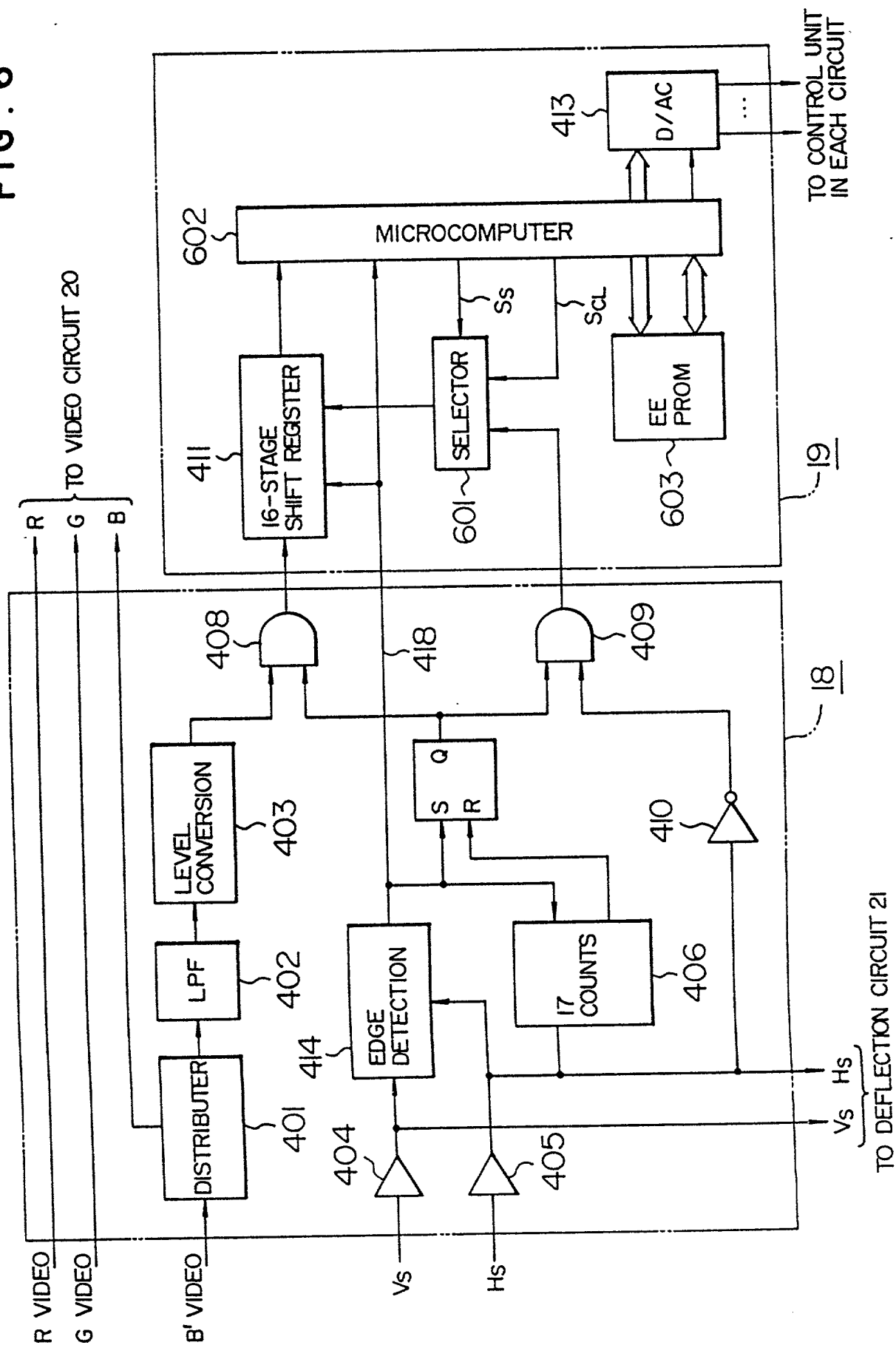


FIG. 7

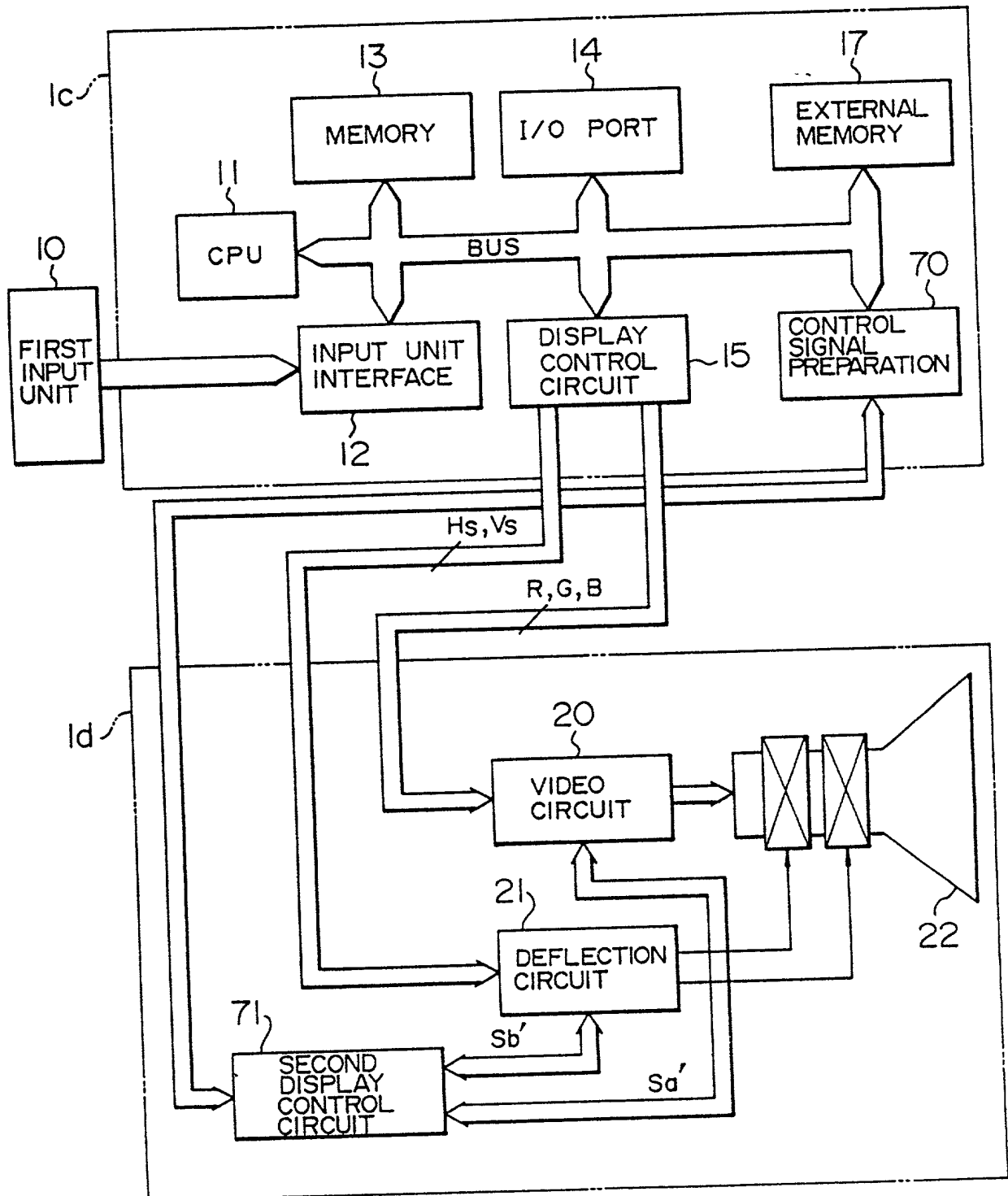


FIG. 8

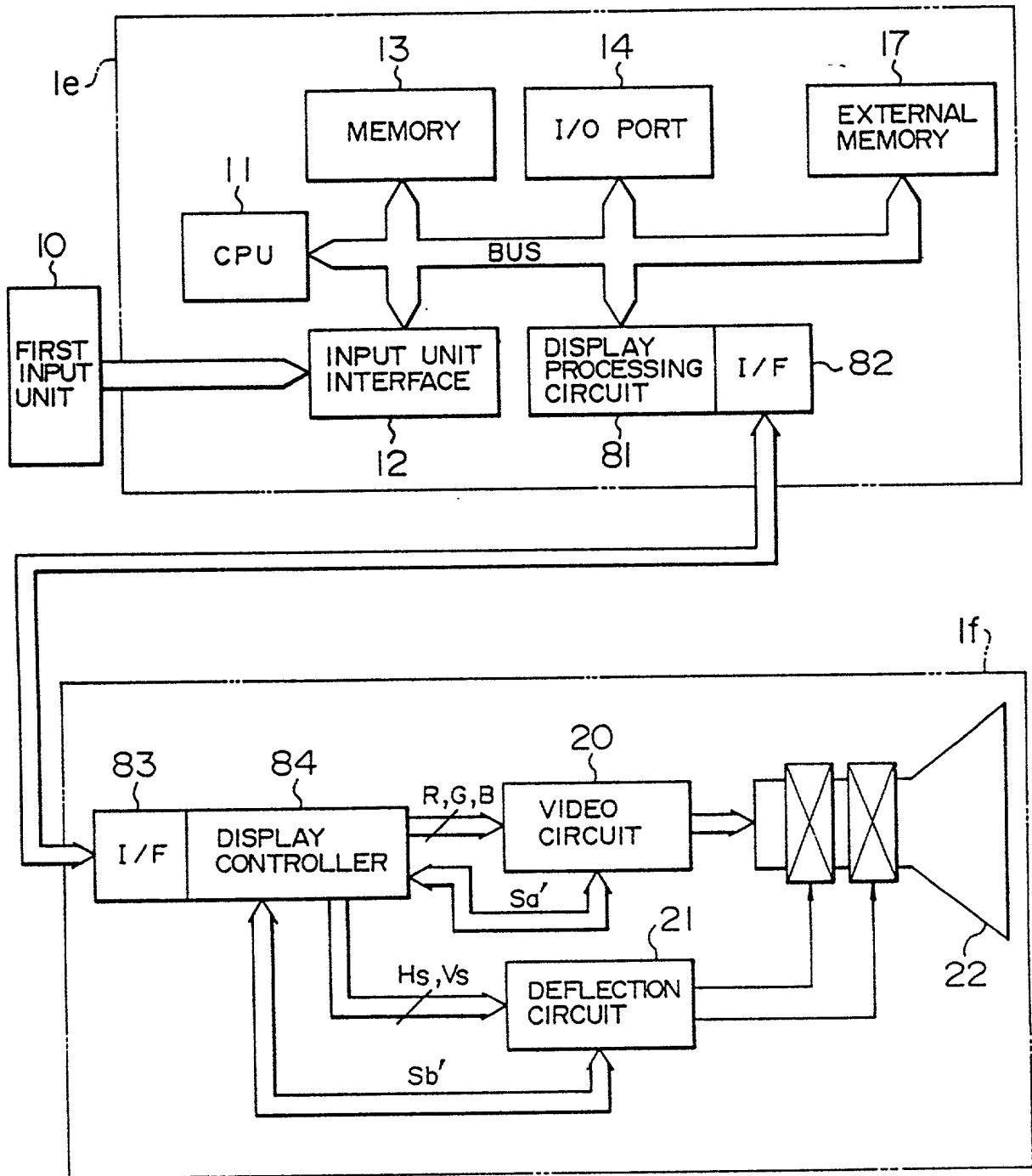


FIG. 9

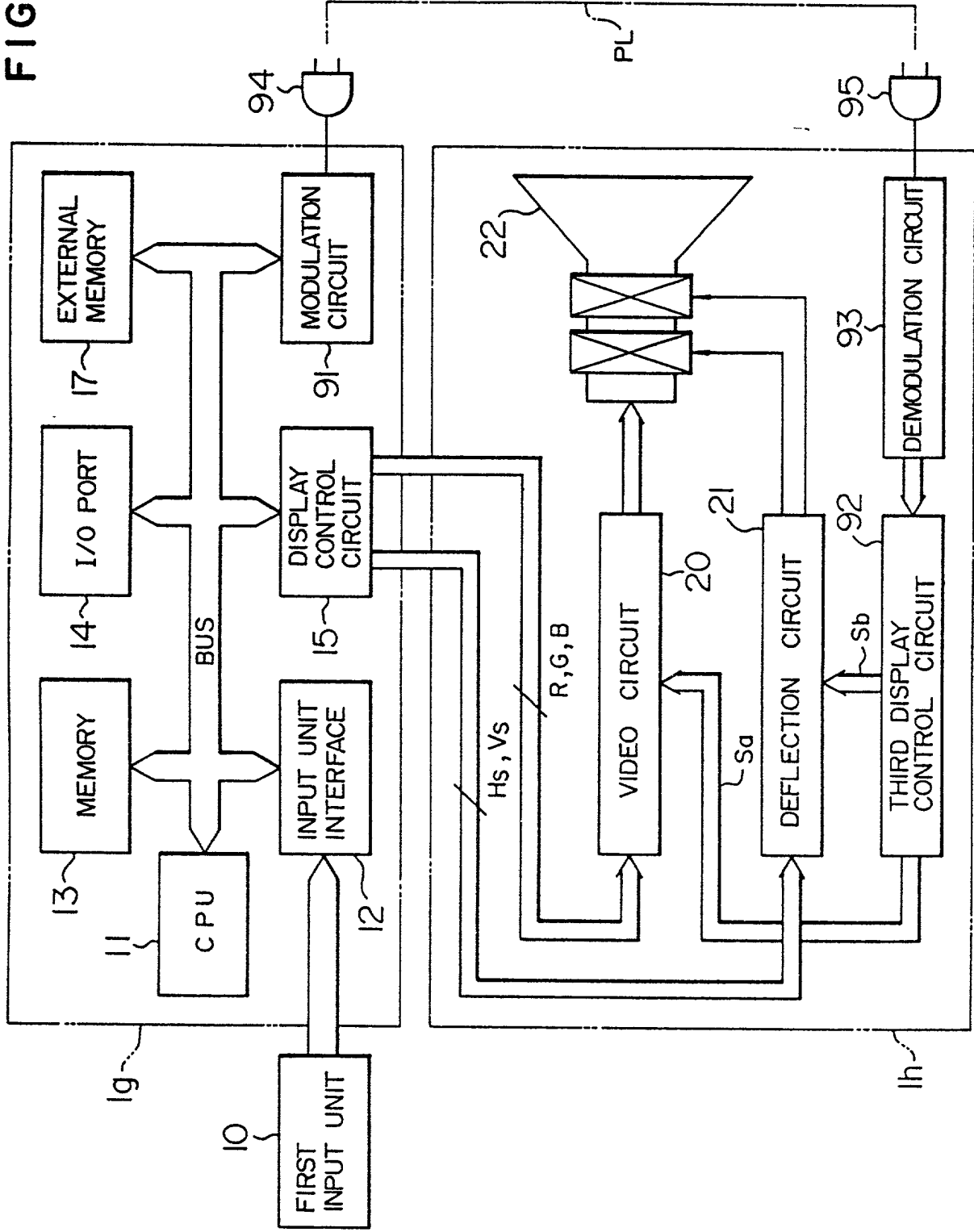
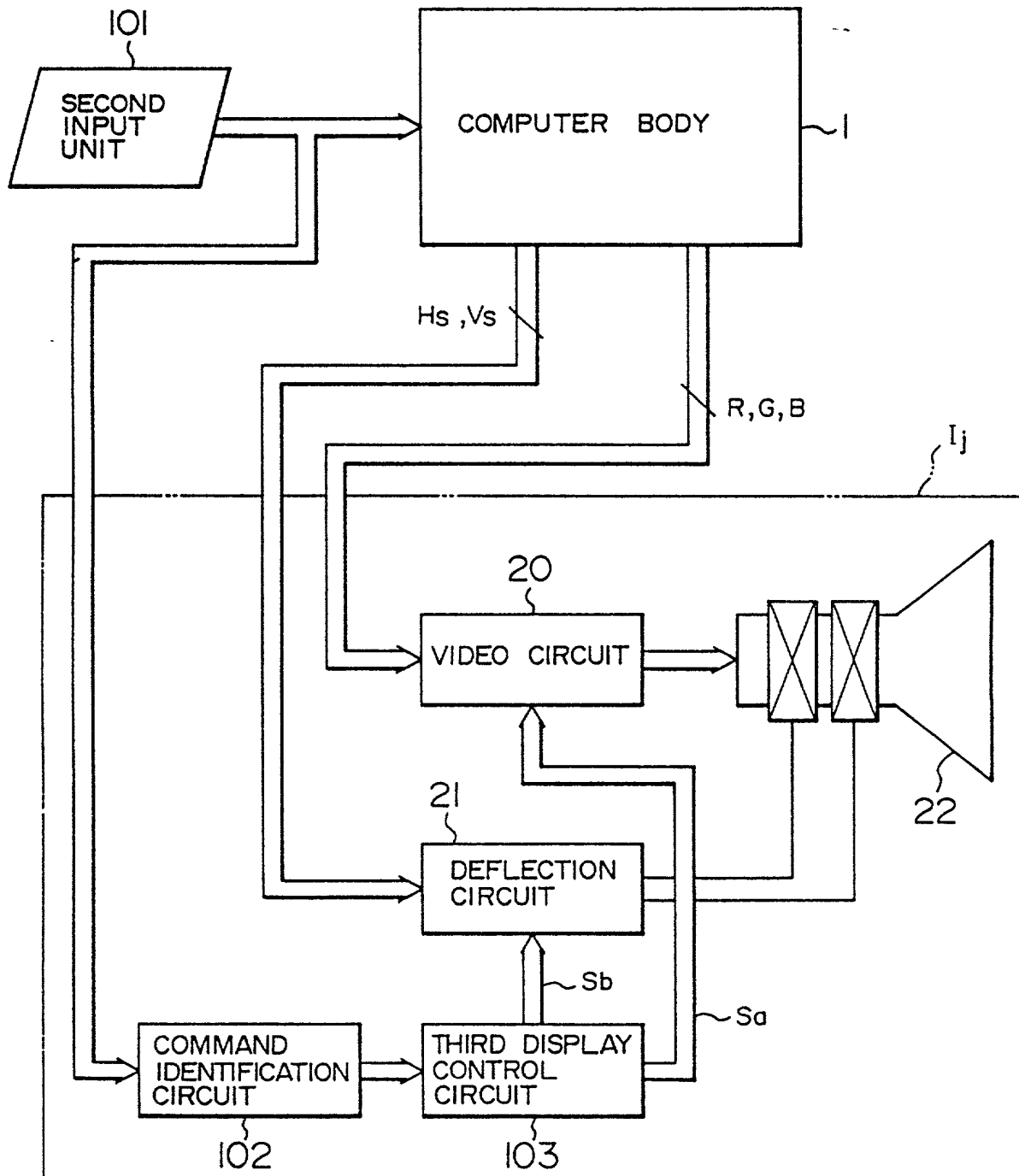


FIG. 10



Declaration and Power of Attorney For Patent Application

特許出願宣言書 Japanese Language Declaration

ATTORNEY'S DOCKET NO.
(IF ANY)

HIT 2 690

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"IMAGE DISPLAY APPARATUS"

その明細書を
(該当する方に印を付す)

the specification of which

(check one)

☐ ここに添付する。

☒ is attached hereto.

☐ _____ 日に出版番号

☐ was filed on _____ as

第 _____ 号として提出し、

Application Serial No. _____

_____ 日に補正した。
(該当する場合)

and was amended on _____
(if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Japanese Language Declaration

私は、合衆国法典第35部第119条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior foreign applications
先の外国出願

Priority claimed
優先権の主張

04-069320	Japan	20 February, 1992
(Number)	(Country)	(Day/Month/Year Filed)
(番号)	(国名)	(出願の年月日)
<hr/>		
(Number)	(Country)	(Day/Month/Year Filed)
(番号)	(国名)	(出願の年月日)
<hr/>		
(Number)	(Country)	(Day/Month/Year Filed)
(番号)	(国名)	(出願の年月日)

<input checked="" type="checkbox"/> Yes あり	<input type="checkbox"/> No なし
<input type="checkbox"/> Yes あり	<input type="checkbox"/> No なし
<input type="checkbox"/> Yes あり	<input type="checkbox"/> No なし

私は、合衆国法典第35部第120条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主項が合衆国法典第35部第112条第1項に規定の様式で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日またはPCT国際出願日の間に公表された連邦規則法典第37部第1章第56条(a)項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)
(出願番号)	(出願日)

(現況)	(Status)
(特許済み、係属中、放棄済み)	(patented, pending, abandoned)

(Application Serial No.)	(Filing Date)
(出願番号)	(出願日)

(現況)	(Status)
(特許済み、係属中、放棄済み)	(patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that those statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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一切の行為を特許商標庁に対して行うことを委任する。
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国籍	CITIZENSHIP Japan		
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	Japan.		
第四の共同発明者氏名		FULL NAME OF FOURTH JOINT INVENTOR IF ANY	
発明者の署名	日付	SIGNATURE	DATE
住所	RESIDENCE		
国籍	CITIZENSHIP		
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